Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Canceled)

2. (Currently Amended) A method of testing an electronic memory device that includes a control logic circuit portion, a matrix array of memory cells, and storage circuitry integrated together on a semiconductor substrate, the method comprising:

loading test data and/or instructions into the control logic circuit portion using a test operation control device, temporarily, said test operation control device being external of, and temporarily connected to, said memory device, said test operation control device having a matrix cell array external to the memory device; and

testing the logic circuit of the memory device by using the external matrix cell array to simulate the matrix array of memory cells of the memory device.

3. (Currently Amended) A method of testing an electronic memory device that includes a control logic circuit portion, a matrix array of memory cells, and storage circuitry integrated together on a semiconductor substrate, the method comprising:

loading test data and/or instructions into the control logic circuit portion using a test operation control device, temporarily, said test operation control device being external of, and temporarily connected to, said memory device, said test operation control device having a control logic external to the memory device; and

testing the matrix array of the memory device by simulating the control logic circuit of the memory device using the external control logic.

4. (Previously Presented) A method according to claim 2 further comprising temporarily connecting the test operation control device to said memory device through data pins and address pins of the memory device, as well as over respective connecting buses.

5. (Previously Presented) A method according to claim 2 wherein said memory array is a non-volatile memory array.

6. (Currently Amended) A control device for testing an electronic memory device formed on a semiconductor substrate, the memory device having a matrix array of memory cells and a control logic circuit portion associated with the memory cell array, as well as circuitry associated with said control logic, the control device comprising:

a memory unit external of and detachably connectable to the memory device, the memory unit configured to ~~operate in substitution of~~simulate the memory cell array during testing of the control logic circuit portion of the memory device.

7. (Original) A device according to claim 6, wherein the detachable connection is established through data pins and address pins of the memory device.

8. (Original) A device according to claim 6, wherein said external memory unit is a non-volatile type.

9. (Original) A device comprising:

an internal memory array integrated onto a semiconductor substrate;

a control logic circuit integrated onto the semiconductor substrate; and

a test control device, external to the semiconductor substrate, having a circuit for simulating the internal memory array to permit testing of the control logic circuit in isolation from the internal memory array.

10. (Previously Presented) The device of claim 9, wherein the test control device includes a circuit for simulating the control logic circuit, the test control device being detachably connectable to the semiconductor substrate.

11. (Original) The device of claim 10, wherein the circuit for simulating the internal memory array and the circuit for simulating the control logic circuit are integrated into one test device.

12. (Original) The device of claim 9, wherein the circuit for simulating the internal memory array is an external memory array.

13. (Original) The device of claim 9, wherein the circuit for simulating the internal memory array comprises a software program in an external memory executed by a testing circuit.

14. (Currently Amended) A method for testing a memory array ~~integrated, with~~ and a control logic circuit~~,~~ integrated onto a semiconductor substrate, comprising:

~~simulating the control logic circuit, using~~ connecting an external ~~connected~~ circuit to the memory device;

performing test operations with the memory array and the external connected circuit, using the external connected circuit to simulate the control logic circuit; and

observing interactions between the memory array and the external connected circuit.

15. (Currently Amended) A method for testing a memory device having a control logic circuit ~~integrated, with~~ and a memory array~~,~~ integrated onto a semiconductor substrate, comprising:

~~simulating the memory array, using~~connecting an external ~~connected~~ circuit to the memory device;

performing test operations with the control logic circuit and the external connected circuit, using the external connected circuit to simulate the memory array; and

observing interactions between the control logic circuit and the external connected circuit.

16. (Currently Amended) A device, comprising:

a semiconductor substrate;

a memory array formed on the substrate;

a control logic circuit formed on the substrate and configured to control operation of the memory array under normal operating conditions; and

bypass circuitry formed on the substrate, and configured to permit substitution of an external memory array configured to simulate the memory array formed on the substrate, for the purpose of testing the control logic circuit separately from the memory array formed on the substrate.

17. (Currently Amended) The device of claim 16, further comprising bypass circuitry formed on the substrate, and configured to permit substitution of an external control logic circuit configured to simulate the control logic circuit formed on the substrate, for the purpose of testing the memory array, separately from the control logic circuit formed on the substrate.

18. (Previously Presented) The device of claim 16 wherein the bypass circuitry comprises an instruction set programmed into the control logic circuit.

19. (Currently Amended) An integrated semiconductor device configured to undergo testing by an external testing device, comprising:

a non-volatile memory array;

a control logic circuit configured to selectively program, read, and erase cells of the non-volatile memory array; and

an instruction set configured to bypass the memory array, such that, when the instruction set is activated, the control logic circuit is configured to program, read, and erase cells of a memory array of the external device, in ~~substitution~~ simulation of the non-volatile memory array.

20. (Currently Amended) The device of claim 19, further comprising an additional instruction set configured to bypass the control logic circuit, such that, when the additional instruction set is activated, the non-volatile memory array is configured to undergo program, read, and erase operations by a control logic of the external testing device, in ~~substitution~~ simulation of the control logic circuit of the integrated semiconductor device.

21. (Previously Presented) The device of claim 19, further comprising a plurality of external pins, and wherein the instruction set is configured to be activated by a command signal at one or more of the external pins of the device.

22. (Currently Amended) An integrated semiconductor device configured to undergo testing by an external testing device, comprising:

a non-volatile memory array;

a control logic circuit configured to selectively program, read, and erase cells of the non-volatile memory array; and

an instruction set configured to bypass the control logic circuit, such that, when the instruction set is activated, the non-volatile memory array is configured to undergo program, read, and erase operations by a control logic of the external testing device, in ~~substitution~~ simulation of the control logic circuit of the integrated semiconductor device.

23. (New) A method according to claim 3 further comprising temporarily connecting the test operation control device to said memory device through data pins and address pins of the memory device, as well as over respective connecting buses.

24. (New) A method according to claim 3 wherein said memory array is a non-volatile memory array.

25. (New) The method of claim 14, further comprising changing control algorithms of circuits integrated onto the semiconductor substrate to couple the external connected circuit with the memory array.

26. (New) The method of claim 15, further comprising changing control algorithms of circuit portions of the memory to couple the external circuit to the control logic circuit.

27. (New) The integrated semiconductor device of claim 22, further comprising an instruction set configured to bypass the memory array, such that, when the instruction set is activated, the control logic circuit is configured to program, read, and erase cells of a memory array of the external device, in simulation of the non-volatile memory array.